

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10750714	
	Filing Date		2003-12-31	
	First Named Inventor		Gonzalez	
	Art Unit		2181	
	Examiner Name		Benjamin P. Geib	
	Attorney Docket Number		PA2683US	

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/BG/	1	6467009		2002-10-15	Winegarten	
/BG/	2	6505241		2003-01-07	Pitts	
/BG/	3	6557092		2003-04-29	Callen	
/BG/	4	6633181		2003-10-14	Rupp	
/BG/	5	6698015		2004-02-24	Moberg	
/BG/	6	6721866		2004-04-13	Roussel	
/BG/	7	6721884		2004-04-13	De Oliveira Kastrup Pereira	
/BG/	8	6732354		2004-05-04	Ebeling	

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/BG/	9	6744274		2004-06-01	Arnold	
/BG/	10	6795900		2004-09-21	Miller	
/BG/	11	6799236		2004-09-28	Dice	
/BG/	12	6817013		2004-11-09	Tabata	
/BG/	13	6831690		2004-12-14	John	
/BG/	14	6857110		2005-02-15	Rupp	
/BG/	15	6874110		2005-03-29	Camarota	
/BG/	16	6883084		2005-04-19	Donohoe	
/BG/	17	6954845		2005-10-11	Arnold	
/BG/	18	6963962		2005-11-06	Ramagopal	
/BG/	19	6968544		2005-11-22	Schneider	

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/BG/	20	6986127		2006-01-10	Newlin	
/BG/	21	6996709		2006-02-07	Arnold	
/BG/	22	7000211		2006-02-14	Arnold	
/BG/	23	7007155		2006-02-28	Mohebbi	
/BG/	24	7062520		2006-06-13	Rupp	
/BG/	25	7086047		2006-08-01	Edwards	
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/BG/	28	7269616		2007-09-11	Rupp	
/BG/	29	7350054		2008-03-25	Furuta	
/BG/	30	7373642		2008-05-13	Williams	

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/BG/	31	7412684		2008-08-12	Gutberlet	
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U.S. PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/BG/	1	20030097546		2003-05-22	Taylor	
/BG/	2	20040193852		2004-09-30	Johnson	
/BG/	3	20040208602		2004-10-21	Plante	

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/BG/	1	0 507 507	EP		1992-07-10	American Telephone		<input type="checkbox"/>
/BG/	2	0 668 659	EP		1995-08-23	Pilkington Germany		<input type="checkbox"/>
/BG/	3	1 443 417	EP		2004-08-04	ST Microelectronics		<input type="checkbox"/>

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/BG/	4	152355	TW		2002-07-10	Adaptive Silicon, Inc.		<input type="checkbox"/>
/BG/	5	152994	TW		2002-07-22	Adaptive Silicon, Inc.		<input type="checkbox"/>
/BG/	6	168210	TW		2003-04-15	Adaptive Silicon, Inc.		<input type="checkbox"/>

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
/BG/	1	RUPP et al.; U.S. Patent Application No. 10/746,018, entitled "Architecture and Method for Reconfigurable Data Path Processing," filed Dec. 23, 2003.	<input type="checkbox"/>
/BG/	2	BECHADE, R.A. et al., "Programmable Arithmetic/Logic Circuits," IBM Technical Disclosure Bulletin, U.S. IBM Corp., New York, Vol. 3, No. 11, April 1981, pp. 4870-4873, XP-000713711.	<input type="checkbox"/>
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/BG/	4	CARRILLO et al.; "The Effect of Reconfigurable Units in Superscalar Processors," 2001; ACM	<input type="checkbox"/>
/BG/	5	DEHON, ANDRE, "Transit Note #118 Notes on Coupling Processors with Reconfigurable Logic," M.I.T. Transit Project, Last Updated March 21, 1995.	<input type="checkbox"/>
/BG/	6	DINIZ, et al., "Automatic Synthesis of Data Storage and Control Structures for FPGA-based Computing Engines," 2000, IEEE, pp 91-100.	<input type="checkbox"/>

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/BG/	7	GONZALEZ, RICARDO E., "Xtensa: A Configurable and Extensible Processor," March-April 2000, IEEE Micro, pp 60-70.	<input type="checkbox"/>
/BG/	8	HENNESSY, JOHN L. and DAVID A. PATTERSON, "Computer Organization and Design: The Hardware/Software Interface," 1998, 2nd edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, p. 345.	<input type="checkbox"/>
/BG/	9	HWANG, KAI, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," 1993, McGraw Hill, pp. 182-183.	<input type="checkbox"/>
/BG/	10	INTEL and HEWLETT-PACKARD, "IA-64 Application Instruction Set Architecture Guide," Revision 1.0, 1999, pp. C-1 through C-3.	<input type="checkbox"/>
/BG/	11	JACOB et al, "Memory Interfacing and Instruction Specification for Reconfigurable Processors," 1999; ACM.	<input type="checkbox"/>
/BG/	12	MIPS Technologies, Inc., "MIPS Extension for Digital Media with 3D," 1996, pp. 1-26.	<input type="checkbox"/>
/BG/	13	RAZDAN, RAHUL and MICHAEL D. SMITH, "A High-Performance Microarchitecture with Hardware-Programmable Functional Units," November 1994, Proc. of MICRO-27, pp. 1-9.	<input type="checkbox"/>
/BG/	14	TANENBAUM, ANDREW S., "Modern Operating Systems," 2001, 2nd edition, Prentice Hall, New Jersey, p. 31.	<input type="checkbox"/>
/BG/	15	TAYLOR, MICHAEL BEDFORD, et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs," Microarchitecture, IEEE Micro, March-April 2002, pp 25-35.	<input type="checkbox"/>
/BG/	16	WAINGOLD, ELLIOT, et al., "Baring It All to Software: Raw Machines," Computer, September 1997, IEEE, pp 86-93.	<input type="checkbox"/>
/BG/	17	YE, Z.A. et al., "CHIMAERA: A high-performance architecture with a tightly-coupled reconfigurable functional unit," June 10-14, 2000, Proc. of the 27th International Symposium on Computer Architecture, pp. 225-235.	<input type="checkbox"/>

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/BG/	18	http://www.tensilica.com/products/xtensa_overview.htm Xtensa Processor Overview	<input type="checkbox"/>
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EXAMINER SIGNATURE

Examiner Signature	/Benjamin Geib/	Date Considered	12/17/2008
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